In the Claims

Please amend Claim **1** and add the following new Claims **2-15**:

1. (*Currently Amended*) A method for ~~rational digital~~ signal synthesis comprising the steps of

providing [[a]] $\underline{N}$ periodic ~~pattern~~ signals each having substantial spectral energy at a frequency f_1;

feeding each of said $\underline{N}$ periodic ~~pattern~~ signals to respectively each of N inputs of an N-way commutator having M commutating sliders, wherein M is at least 2 but no greater than N ; and

~~clocking the periodic pattern generator at a frequency f1; and~~

rotating the M commutator sliders across the N inputs of the N-way commutator at a frequency f_2, thereby obtaining at each of the M commutator sliders an output signal having substantial spectral energy at an output frequency $\underline{f_0}$ ~~of~~ [[$f_1 \pm f_2$]] wherein $f_0 = f_2 + f_1$ or $f_0 = f_2 - f_1$.

2. (*New*) A method for signal synthesis comprising the steps of Claim **1** and further comprising the steps of

feeding each of the output signals obtained at each of said M commutator sliders to respectively each of M inputs of an M-way commutator having L commutating sliders, wherein L is less than or equal to M; and

rotating the L commutator sliders of said M-way commutator across the M inputs of said M-way commutator at a frequency f_3, thereby obtaining at each

of the L commutator sliders an output signal having substantial spectral energy at an output frequency f_4 wherein $f_4 = f_3 + f_0$ or $f_4 = f_3 - f_0$.

3. (*New*) A signal synthesizer comprising

a generator for generating N periodic signals each having substantial spectral energy at a frequency f_1;

an N-way commutator having N inputs and M commutating sliders, wherein M is at least 2 but no greater than N and wherein each of said N periodic signals are respectively coupled to each of the N inputs of said N-way commutator;

an arrangement for rotating the M commutator sliders of said N-way commutator across the N inputs of said N-way commutator at a frequency f_2, thereby obtaining at each of the M commutator sliders an output signal having substantial spectral energy at an output frequency f_0 wherein $f_0 = f_2 + f_1$ or $f_0 = f_2 - f_1$.

4. (*New*) A signal synthesizer comprising a first synthesizer in accordance with Claim **3** and further comprising

an M-way commutator having L commutating sliders, wherein L is less than or equal to M and wherein each of said M sliders of said first synthesizer are respectively coupled to each of the M inputs of said M-way commutator;

an arrangement for rotating the L commutator sliders of said M-way commutator across the M inputs of said M-way commutator at a frequency f_3, thereby obtaining at each of the L commutator sliders an output signal having

substantial spectral energy at an output frequency f_4 wherein $f_4 = f_3 + f_0$ or $f_4 = f_3 - f_0$.

5. (*New*) A signal synthesizer in accordance with Claim **3** wherein N=4.

6. (*New*) A signal synthesizer in accordance with Claim **4** wherein M=4

7. (*New*) A signal synthesizer in accordance with Claim **6** wherein N=4

8. (*New*) A signal synthesizer in accordance with Claim **3** further comprising

   a weighting filter producing a filtered output signal and having inputs that are coupled to at least two of the M commutator sliders; and

   wherein the input weighting values of said weighting filter are set so that the filtered output signal has an improved spectral purity about the output frequency f_0.

9. (*New*) A signal synthesizer in accordance with Claim **4** wherein L is at least 2 further comprising

   a weighting filter producing a filtered output signal and having inputs that are coupled to at least two of the L commutator sliders; and

   wherein the input weighting values of said weighting filter are set so that the filtered output signal has an improved spectral purity about the output frequency f_4.

10. (*New*) A phased lock loop signal synthesizer having a reference signal input coupled to the filtered output signal of the synthesizer of Claim **8**.

11. (*New*) A phased lock loop signal synthesizer having a reference signal input coupled to the filtered output signal of the synthesizer of Claim **9**.

12. (*New*) An injection locked oscillator (ILO) having an injection reference signal input coupled to the filtered output signal of the synthesizer of Claim **8**.

13. (*New*) An injection locked oscillator (ILO) having an injection reference signal input coupled to the filtered output signal of the synthesizer of Claim **9**.

14. (*New*) A phase lock loop having a differential input feedback loop filter, said phase lock loop further comprised of

a ternary level phase detector having one oscillator input line, two reference input lines and two output lines coupled to the differential input feedback loop filter; and

a ternary level reference signal generator comprised of a signal synthesizer in accordance with Claim **3** wherein M=2 and wherein the two commutator sliders produce output signals representative of a ternary signal; and

wherein said two commutator sliders are coupled to the two reference input lines of said ternary level phase detector.

15. (*New*) A phase lock loop having a differential input feedback loop filter, said phase lock loop further comprised of

a ternary level phase detector having one oscillator input line, two reference input lines and two output lines coupled to the differential input feedback loop filter; and

a ternary level reference signal generator comprised of a signal synthesizer in accordance with Claim **4** wherein *L*=2 and wherein the *L* commutator sliders produce output signals representative of a ternary signal; and

wherein said *L* commutator sliders are coupled to the two reference input lines of said ternary level phase detector.